What is laim d is:

1. An asynchronous switching mode voltage regulator comprising:

an output stage connected between an input voltage and a reference potential for generating an output voltage, said output stage including a switch connected between said input voltage and a phase node, and an unidirectional current-conducting device connected between said phase node and reference potential;

a pulse width modulator responsive to said output voltage for generating a PWM signal; and

an adjustable one-shot circuit connected with an adjustable voltage for generating an adjustable signal at a light loading to adjust an ON duty of said switch.

2. The regulator according to claim 1, wherein said unidirectional current-conducting device comprises a diode.

3. The regulator according to claim 1, wherein said adjustable one-shot circuit comprises:

a charger;

a flip-flop connected with said PWM signal for generating

said adjustable signal to control said charger to be charged and discharged;

a charging current generator connected with said input voltage and adjustable voltage for providing a charging current to charge said charger to thereby generate a charger output; and

a comparator for comparing said charger output with a reference voltage to generate a reset signal to reset said flip-flop.

4. The regulator according to claim 3, wherein said charging current generator comprises:

a current source connected with said input voltage for generating a first current;

a current mirror having a reference branch connected with said first current and a mirror branch for generating a mirrored current by mirroring said first current; and

a current sink connected with said mirror branch and adjustable voltage for separating a second current from said mirrored current to thereby determine said charging current.

5. The regulator according to claim 4, wherein said first current is proportional to said input voltage.

6. The regulator according to claim 4, wherein said second current is proportional to said adjustable voltage.

7. The regulator according to claim 1, wherein said adjustable voltage is proportional to said output voltage.

8. A method for efficiency improvement of an asynchronous switching mode voltage regulator including an output stage connected between an input voltage and a reference potential for generating an output voltage, said output stage having a switch connected between said input voltage and a phase node, and an unidirectional current-conducting device connected between said phase node and reference potential, and a pulse width modulator responsive to said output voltage for generating a PWM signal, said method comprising the steps of:

generating an adjustable signal upon an adjustable voltage at a light loading; and

adjusting an ON duty of said switch by said adjustable signal.

9. The method according to claim 8, wherein said step of generating an adjustable signal comprises the steps of:

triggering a flip-flop to generate a flip-flop output by said PWM signal;

generating said adjustable signal in response to said flip-flop output;

generating a charging current;

charging a charger by said charging current and discharging said charger under control of said flip-flop output to thereby generate a charger output; and

comparing said charger output with a reference voltage to generate a reset signal to reset said flip-flop.

10. The method according to claim 9, wherein said step of generating a charging current comprises the steps of:

generating a first current proportional to said input voltage;

generating a mirrored current by mirroring said first current; and

separating a second current proportional to said adjustable voltage from said mirrored current for determining said charging current.

11. The method according to claim 8, further comprising controlling said adjustable voltage proportional to said output voltage.

12. A synchronous switching mode voltage regulator

comprising:

an output stage connected between an input voltage and a reference potential for generating an output voltage, said output stage including a high-side switch connected between said input voltage and a phase node, and a low-side switch connected between said phase node and reference potential;

a pulse width modulator responsive to said output voltage for generating a PWM signal;

a phase detector for detecting a voltage on said phase node to generate a detection signal to block said low-side switch at a light loading;

an adjustable one-shot circuit connected with an adjustable voltage for generating an adjustable signal by triggered by said detection signal;

a control signal responsive to said adjustable signal for adjusting an ON duty of said high-side switch at said light loading; and

an OFF duty detector for resetting said phase detector when said regulator escapes from said light loading.

13. The regulator according to claim 12, wherein said phase detector comprises:

a comparator for comparing said voltage on said phase node and reference potential to generate a

comparison signal; and

a flip-flop responsive to said control signal and comparison signal for generating said detection signal.

14. The regulator according to claim 12, wherein said adjustable one-shot circuit comprises:

a charger;

a flip-flop connected with said PWM signal for generating said adjustable signal to control said charger to be charged and discharged;

a charging current generator connected with said input voltage and adjustable voltage for providing a charging current to charge said charger to thereby generate a charger output; and

a comparator for comparing said charger output with a reference voltage to generate a reset signal to reset said flip-flop.

15. The regulator according to claim 14, wherein said charging current generator comprises:

a current source connected with said input voltage for generating a first current;

a current mirror having a reference branch connected with said first current and a mirror branch for

generating a mirrored current by mirroring said first current; and

a current sink connected with said mirror branch and adjustable voltage for separating a second current from said mirrored current to thereby determine said charging current.

16. The regulator according to claim 15, wherein said first current is proportional to said input voltage.

17. The regulator according to claim 15, wherein said second current is proportional to said adjustable voltage.

18. The regulator according to claim 12, wherein said OFF duty detector comprises:

a next clock generator for generating a next clock signal by delaying said control signal; and

a reset signal resulted from said control signal and next clock signal for resetting said phase detector.

19. The regulator according to claim 18, wherein said next clock generator comprises:

a first flip-flop connected with said control signal for generating a first signal;

a second flip-flop connected with a clock signal and said

first signal for generating said next clock signal; and

an AND gate connected with said next clock signal and an inverse of said clock signal for generating said reset signal to reset said first and second flip-flops.

20. A method for efficiency improvement of a synchronous switching mode voltage regulator including an output stage connected between an input voltage and a reference potential for generating an output voltage, said output stage having a high-side switch connected between said input voltage and a phase node, and a low-side switch connected between said phase node and reference potential, and a pulse width modulator responsive to said output voltage for generating a PWM signal, said method comprising the steps of:

detecting a voltage on said phase node for generating a detection signal to block said low-side switch at a light loading;

generating an adjustable signal upon said detection signal and an adjustable voltage;

generating a control signal in response to said adjustable signal for adjusting an ON duty of said high-side switch at said light loading; and

generating a reset signal for resetting said detection signal when said regulator escapes from said light

loading.

21. The method according to claim 20, wherein said step of generating an adjustable signal comprises the steps of:

triggering a flip-flop to generate a flip-flop output by said PWM signal;

generating said adjustable signal in response to said flip-flop output;

generating a charging current;

charging a charger by said charging current and discharging said charger under control of said flip-flop output to thereby generate a charger output; and

comparing said charger output with a reference voltage for generating said reset signal to reset said flip-flop.

22. The method according to claim 21, wherein said step of generating a charging current comprises the steps of:

generating a first current proportional to said input voltage;

generating a mirrored current by mirroring said first current; and

separating a second current proportional to said adjustable voltage from said mirrored current for

determining said charging current.

23. The method according to claim 20, further comprising controlling said adjustable voltage proportional to said output voltage.

24. The method according to claim 20, wherein said step of generating a reset signal comprises the steps of:

generating a next clock signal by delaying said control signal; and

generating said reset signal upon said control signal and next clock signal.